REMARKS

The enclosed is responsive to the Office Action mailed on November 29, 2005. At the time the Office Action was mailed, claims 18-24 were pending. By way of the present response the Applicant has: 1) amended claims 18-24, 2) added claims 25-37; and 3) canceled no claims. As such, claims 18-37 are now pending. The Applicant respectfully requests reconsideration of the present application and allowance of all claims now presented

Claim Rejections

Claim 18 is an independent claim. Claims 19-24 depend directly or indirectly from claim 18.

The Office Action rejected claims 18-20, 22 and 24 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,846,853 by Otsuki et al. (hereinafter "*Otsuki*"). The Office Action rejected claim 21under 35 U.S.C. § 103(a) as being unpatentable over *Otsuki* as applied to claims 18-20, 22 and 24 above, and further in view of U.S. Publication No. 2003/0138553 A1 by Takenaka et al. (hereinafter "*Takenaka*"). The Office Action rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over *Otsuki* as applied to claims 18-20, 22 and 24 above, and further in view of U.S. Publication No. 2004/0212030 A1 by Asai et al. (hereinafter "*Asai*"). The Applicant respectfully traverses.

Independent claim 18 now recites the limitation of: "a layer of nonconductive compliant material...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures." The Applicant respectfully submits that none of the above references disclose or suggest this limitation.

As can be understood with reference to *Otsuki*'s figures, *Otsuki* does not disclose or suggest a layer of nonconductive compliant material, at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures.

The photosensitive resin 7 of *Otsuki* is not a layer of nonconductive compliant material, at least a portion of which has a top surface lower than a top surface of at least one of said first plurality of interconnect structures. The photosensitive resin 7 of *Otsuki* is conductive. *Otsuki* describes: "the positive type photosensitive resin [7] including conductive particulates 3 is painted on the surface of the mounting portion of the liquid crystal display panel 1." (*Otsuki*, col. 3, lines 32-33, emphasis added). In *Otsuki*, "the electrode 2 of the liquid crystal display panel 1 and the electrode of the liquid crystal driving IC 4 electrically contact through the conductive particulates 3" of the photosensitive resin 7. (*Otsuki*, col. 3, lines 55-57, emphasis added). Therefore, the photosensitive resin 7 of *Otsuki* is not a layer of nonconductive compliant material, at least a portion of which has a top surface lower than a top surface of at least one of said first plurality of interconnect structures.

Additionally, neither the ultraviolet curing resin 6 nor the photosensitive resin 17 of *Otsuki* is a layer of nonconductive compliant material, at least a portion of which has a top surface lower than a top surface of at least one of said first plurality of interconnect structures. As can be understood with reference to the *Otsuki*'s figures, neither the ultraviolet curing resin 6 nor the photosensitive resin 17 is has a top surface which is lower than a top surface of electrode 2 (the asserted "interconnect structure", see Office Action p. 2).

Therefore, neither the photosensitive resin 7, nor the ultraviolet curing resin 6, nor the photosensitive resin 17 of *Otsuki* is a layer of nonconductive compliant material, at least a portion of which has a top surface lower than a top surface of at least one of said first plurality of interconnect structures.

Therefore, *Otsuki* does not disclose or suggest the limitation of "at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures" as required by claim 18.

Takenaka also does not disclose or suggest this limitation missing from *Otsuki*. *Takenaka* describes a "method of manufacturing multi-layer circuit board comprising: a hole forming step for forming through-holes or blind-holes in a plate-form or sheet-form board material, and a filling step for filling a paste into through-holes or blind-holes formed in the hole forming step by using a filling means." (*Takenaka*, Abstract).

Takenaka does not disclose or suggest "a layer of nonconductive compliant material...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures" as required by claim 18.

Asai also does not disclose or suggest this limitation missing from *Otsuki* and *Takenaka*. *Asai* describes "a device for optical communication comprising: a substrate for mounting an IC chip having a light emitting element and a light receiving element mounted at predetermined positions; and a multilayered printed circuit board having an optical waveguide formed at a predetermined position, which is low in connection loss among the mounted optical components and which has excellent connection reliability." (*Asai*, Abstract). *Asai* describes examples of various resins. (See *Asai*, paragraphs 257-262).

Asai does not disclose or suggest "a layer of nonconductive compliant material...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures" as required by claim 18.

Yoshida (U.S. Publication No. 2003/0098700), cited by the Office Action as evidence that LCD contains silicon, also does not disclose or suggest this limitation missing from *Otsuki*, *Takenaka*, and *Asai*. *Yoshida* describes "a probe card apparatus and a probe used therefor providing satisfactory electrical contact with a prescribed electrode portion formed on a semiconductor chip and the like, when a plurality of semiconductor chips formed on a silicon wafer is subjected to an electrical test such as a circuit test, in the form of a wafer, or when circuit elements such as liquid crystal display panels (LCD) and the like are subjected to electrical circuit test." (*Yoshida*, Technical Field).

Yoshida does not disclose or suggest "a layer of nonconductive compliant material...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures" as required by claim 18.

Therefore, none of the cited references, individually or in combination, disclose or suggest the limitation required by claim 18 of "a layer of nonconductive compliant material...at least a portion of the layer of nonconductive compliant material having a top surface lower than a top surface of at least one of said first plurality of interconnect structures."

Therefore, claim 18 is patentable over the cited references. Claims 19-24 depend directly or indirectly from claim 18. Therefore, claims 19-24 are also patentable over the cited references for at least the foregoing reasons.

Accordingly, the Applicant respectfully requests withdrawal of the rejections of claims 18-20, 22 and 24 under 35 U.S.C. § 102(b) as being anticipated by *Otsuki*, the rejection of claim 21 under 35 U.S.C. §103(a) as being unpatentable over *Otsuki*, and further in view of *Takenaka*, and the rejection of claim 23 under 35 U.S.C. § 103(a) as being unpatentable over *Otsuki* and further in view of *Asai*.

New Claims

The Applicant respectfully submits that the new claims are in condition for allowance.

New independent claims 25, 32 and 35 each claim a stacked wafer structure. *Otsuki*, *Takenaka*, *Asai*, and *Yoshida* do not, individually or in combination, disclose or suggest a stacked wafer structure.

Otsuki describes a "method which connects the semiconductor parts or sub-circuit substrates to the electrodes formed on the main circuit substrate. For example, the method is used for connecting a liquid-crystal driving IC, a glass substrate or a film carrier substrate which mounts electric parts such as an IC chip thereon to the electrodes formed on the liquid crystal panel." (*Otsuki*, col. 1, lines 13-19).

Otsuki does not disclose or suggest a stacked wafer structure.

Takenaka describes "a method of manufacturing circuit boards used for various electronic equipment, and a circuit board manufacturing apparatus." (*Takenaka*, Technical Field). *Takenaka* does not disclose or suggest a stacked wafer structure.

Asai describes "a substrate for mounting an IC chip, a multilayered printed circuit board and a device for optical communication." (*Asai*, Technical Field). *Asai* does not disclose or suggest a stacked wafer structure.

Yoshida describes "a probe card apparatus and a probe used therefore." (*Yoshida*, Technical Field). *Yoshida* does not disclose or suggest a stacked wafer structure.

Therefore, *Otsuki*, *Takenaka*, *Asai*, and *Yoshida* do not, individually or in combination, disclose or suggest a stacked wafer structure. Therefore, new independent claims 25, 32 and 35, and the claims which depend therefrom, are each patentable over *Otsuki*, *Takenaka*, *Asai*, and *Yoshida* for at least the foregoing reason.

CONCLUSION

The Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Ms. Van N. Nguy or Mr. Michael Bernadicou at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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